a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is configured to receive data during time periods of predetermined length; where the control circuit is configured to place at least a minimum amount of data from the first queue onto the bus during each time period; where the control circuit is configured to place data from the second queue onto the bus only when the bus is otherwise unoccupied.

4. (Amended) The system of claim 3, where the peripheral device includes a network interface component connected to receive the data from a computer network.

5. (Amended) The system of claim 3, wherein the data includes packetized voice data.

6. (Amended) A computer system comprising:

a host processor;

a peripheral device configured to transfer data to the host processor over an attachment bus using at least first and second types of data transfers, comprising:

a classifying circuit configured to separate the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer;

a first queue connected to receive the first class of data from the classifying circuit;

a second queue connected to receive the second class of data from the classifying circuit; and

a control circuit configured to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is a Universal Serial Bus (USB) and the peripheral device is configured to transfer data over the bus using isochronous and bulk transfers.

B3

7. (Amended) The system of claim 3, where the peripheral device is configured to deliver the data in packets of predetermined length.

8. (Amended) The system of claim 7, where the classifying circuit is configured to place each of the packets into one of the queues.

9. (Amended) The system of claim 7, where a portion of each packet indicates a channel associated with the packet, and where the classifying circuit includes a storage device that stores information indicating each of the channels that is associated with at least one of the classes.

10. (Amended) The system of claim 9, where the classifying circuit includes a selection element configured to compare, for each packet, the information in the storage device to the data in the portion of the packet that

indicates the channel and configured to select a corresponding one of the queues to receive the packet.

13. (Amended) A method comprising:

transferring data to a host processor over an attachment bus using at least first and second types of data transfers and, in transferring the data:

separating the data into a first class associated with the first type of transfer and a second class associated with the second type of transfer; and

placing data of the first class onto the bus at a higher priority than data of the second class is placed onto the bus.

placing data on the bus during time periods of predetermined length, where placing data of the first class on the bus includes placing at least a minimum amount of data of the first class onto the bus during each time period; and

placing data of the second class onto the bus only when the bus is otherwise unoccupied.

14. (Amended) The method of claim 13, further comprising receiving the data from a computer network.

15. (Amended) The method of claim 13, where receiving the data includes receiving packetized voice data.

16. (Amended) The method of claim 13, where transferring data includes delivering the data in packets of predetermined length.

17. (Amended) The method of claim 11, where separating the data includes placing each of the packets into one of the queues.

18. (Amended) The method of claim 11, further comprising storing information indicating each channel that is associated with at least one of the classes.

19. (Amended) The method of claim 18, further comprising:

comparing, for each packet, the stored information to a portion of the data in the packet that indicates the channel associated with the packet; and

placing the packet into a corresponding one of the queues.

Please add the following new Claims 20-24:

20. (New) The system of claim 9, where the classifying circuit comprises a buffer, a shift register and a content addressable memory (CAM) device.

21. (New) The system of claim 3, wherein the bus is a Peripheral Component Interface (PCI) bus.

22. (New) The system of claim 3, wherein the bus uses an Asynchronous Transfer Mode (ATM).

23. (New) A peripheral device coupled between a host device and a network, the peripheral device operable to

transfer data packets to the host processor over a bus, the peripheral device comprising:

a classifying circuit operable to identify a priority level of each data packet from the network;

a first queue operable to store data packets with a first priority level from the classifying circuit;

a second queue operable to store data packets with a second priority level from the classifying circuit; and

a control circuit coupled to first and second queues, the control circuit being operable to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is configured to receive data during time periods of predetermined length; the control circuit being configured to place at least a minimum amount of data from the first queue onto the bus during each time period; the control circuit being configured to place data from the second queue onto the bus only when the bus is otherwise unoccupied.

24. (New) A peripheral device coupled between a host device and a network, the peripheral device operable to transfer data packets to the host processor over a bus, the peripheral device comprising:

a classifying circuit operable to identify a priority level of each data packet from the network;

a first queue operable to store data packets with a first priority level from the classifying circuit;

a second queue operable to store data packets with a second priority level from the classifying circuit; and

B3

a control circuit coupled to first and second queues, the control circuit being operable to place data from the first queue onto the bus at a higher priority than data from the second queue is placed onto the bus;

where the bus is a Universal Serial Bus (USB) and the peripheral device is configured to transfer data over the bus using isochronous and bulk transfers.